22nm HP Integrated Patterning Improvements for EUVL

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Intel Corporation

Oct 20, 2010

SEMATECH EUV Focus Areas 2005-2009: 22 nm half-pitch insertion target*

2005 / 32hp	2006 / 32hp	2007 / 22hp**	2008 / 22hp	2009 / 22hp
1. Resist resolution, sensitivity & LER met simultaneously	1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure
2. Collector lifetime	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF
3. Availability of defect free mask	3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Source power	4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration
• Reticle protection during storage, handling and use	5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime	
• Projection and illuminator optics quality & lifetime				

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*2009 EUVL Symposium, SEMATECH
** 2007 focus was still 32 nm hp

Logic Technology Nodes

Process Name	P1266	P1268	P1270	P1272	P1274
1st Production	2007	2009	2011	2013	2015
Logic Tech. node*	45 nm	32 nm	22 nm	15 nm	11 nm

Current integrated test chips

EUV pilot line in 2011

Manufacturing

Development

Pathfinding

Research

*** Logic technology node has no correspondence to half pitch**

Intel's 11nm Node - 2015 HVM*

193i with Pitch Division can and will be extended as viable option for Intel's 11nm Node patterning in 2015

	32nm	22nm	15nm	11nm
Min Pitch	112.5nm	*0.71	*0.71	*0.71 = 40nm

Still Single Pitch Division, might need 5 masks for complex dense 2D layouts.

***ITRS 2008 Reference*:**

Year of Production	2013	2015	2017	2019	2021
MPU Metal 1 Pitch *nm*	64	50	40	31.8	25.2

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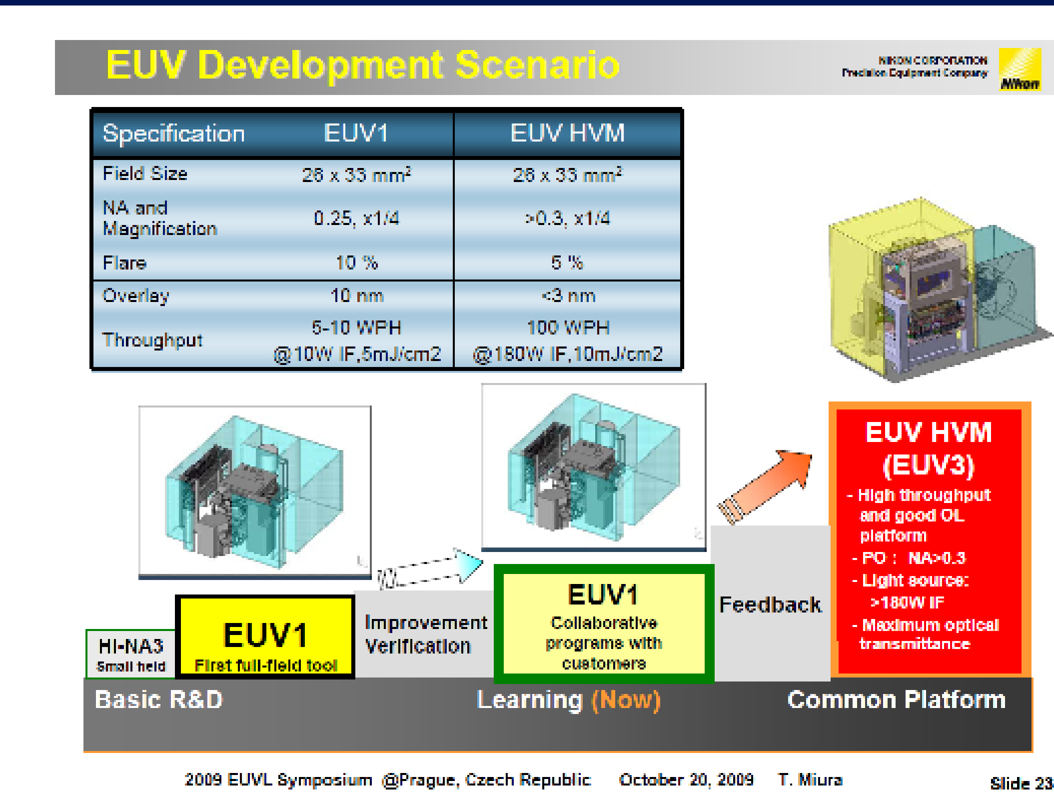
*Y. Borodovsky, Intel Corporation, 2009 SEMICON West

Outline

What do we need to address 22 nm hp integrated process development using EUVL?

- Tools
- Resist
- Corrections
  - EUV specific

EUV HVM tool roadmaps have higher NA


EUV Development Scenario

Specification	EUV1	EUV HVM
Field Size	26 x 33 mm²	26 x 33 mm²
NA and Magnification	0.25, x1/4	>0.3, x1/4
Flare	10 %	5 %
Overlay	10 nm	<3 nm
Throughput	5-10 WPH @10W IF,5mJ/cm2	100 WPH @180W IF,10mJ/cm2

"ASML EUV Program: Status and Prospects", J. Benschop, 2009 EUVL Symposium

"Nikon EUVL Development Progress Update", T. Miura, 2009 EUVL Symposium

- >0.3 NA tools are planned for HVM
- Though initial development will be done with 0.25 NA tools

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EUV exposure tools: MET, EUV1, ADT**

Process transfer

Intel MET

EUV1

IMEC ADT

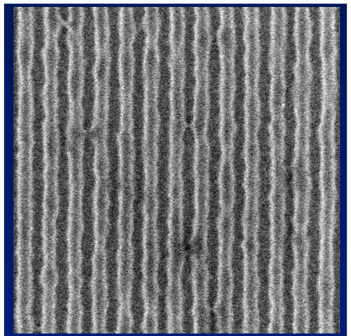
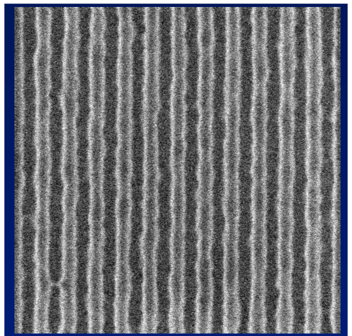
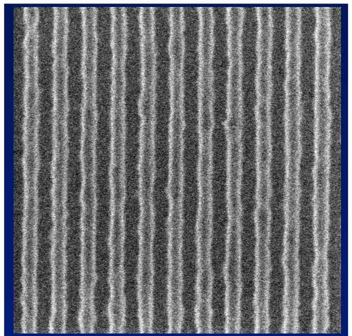
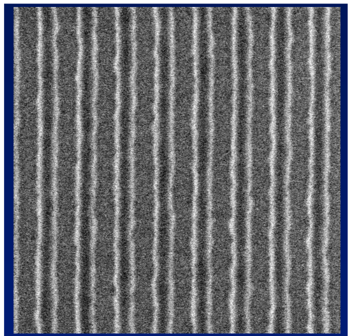
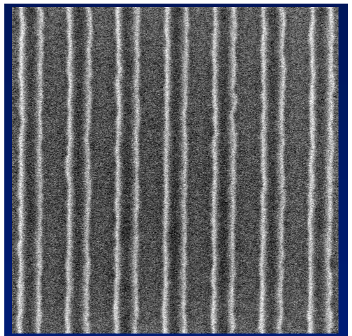
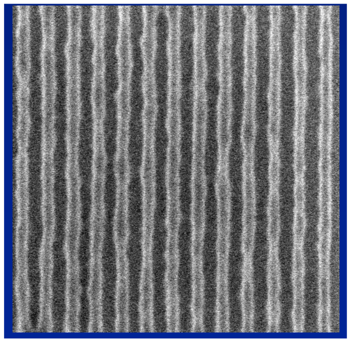
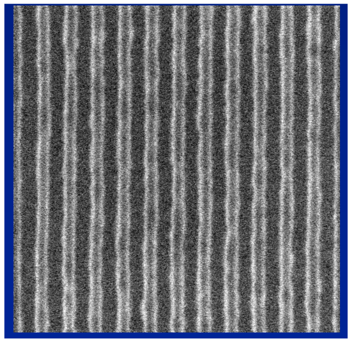
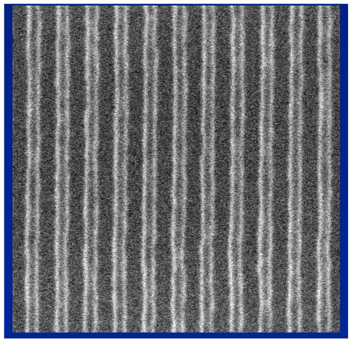
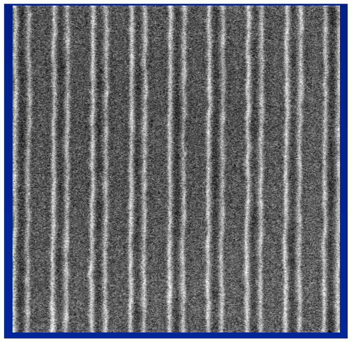
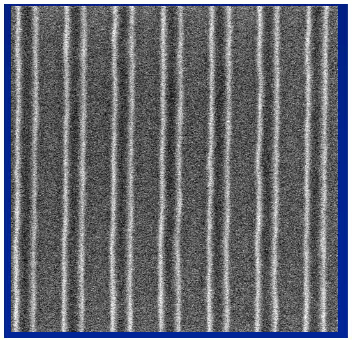
0.25 NA resolution concerns for 22 nm hp

	Intel MET	Nikon EUV1	ADT
Field size	600 x 600 μm^2	26 x 33 mm^2	26 x 33 mm^2
NA	0.30*	0.25	0.25
Illumination	0.36/0.68 annular/quad/dipole	Max. 0.8 sigma + OAI	0.5 disk
Flare	~4%	~8%	~16%
Overlay	No	Yes	Yes

*with 10% area central obscuration

** G. Vandentop, SPIE 2009

Observe LWR improvement in move from MET → IMEC ADT*

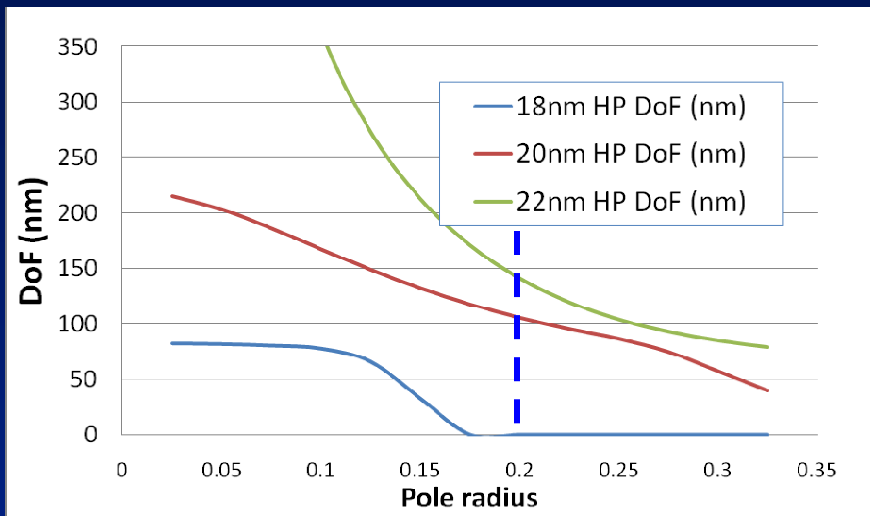
	26 nm HP	28 nm HP	30 nm HP	40 nm HP	50 nm HP
Intel MET (quad) Esize ~ 14.5 mJ/cm^2					
LWR	6.9	4.8	4.9	4.6	4.1
IMEC ADT Esize ~ 13.0 mJ/cm^2					
LWR	5.9	4.6	3.6	3.1	2.4
	- 14 %	- 5 %	- 26 %	- 33 %	- 40 %

Side-by-side comparison indicates ADT can yield ~ 25% lower LWR than Intel MET

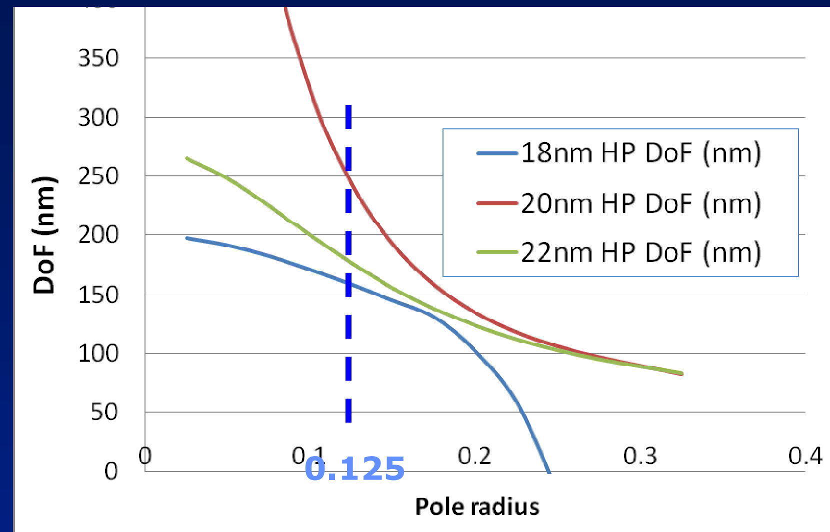
***2010 EUVLS poster – Putna et al**

How to squeeze the most out of 0.25 NA tools? – Dipole and Alt. PSM

Dipole Center=0.60



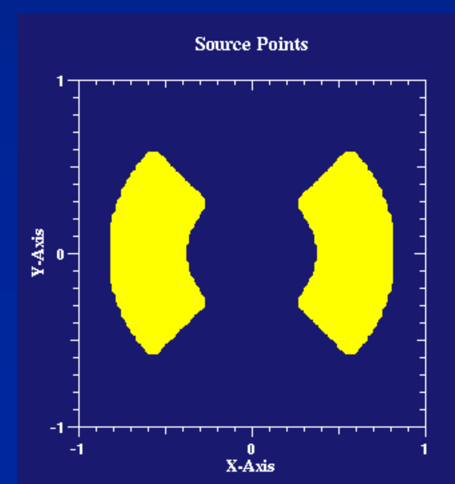
Dipole center=0.675



$\sigma_{max} \leq 0.8$

$$P\_opt = \frac{\lambda}{2 * P * NA}$$

- Aerial image modeling of line/space patterns
- DoF based on contrast > 60%
- Optimum pole center for < 22nm HP = 0.675
- Dipole angle optimized for throughput



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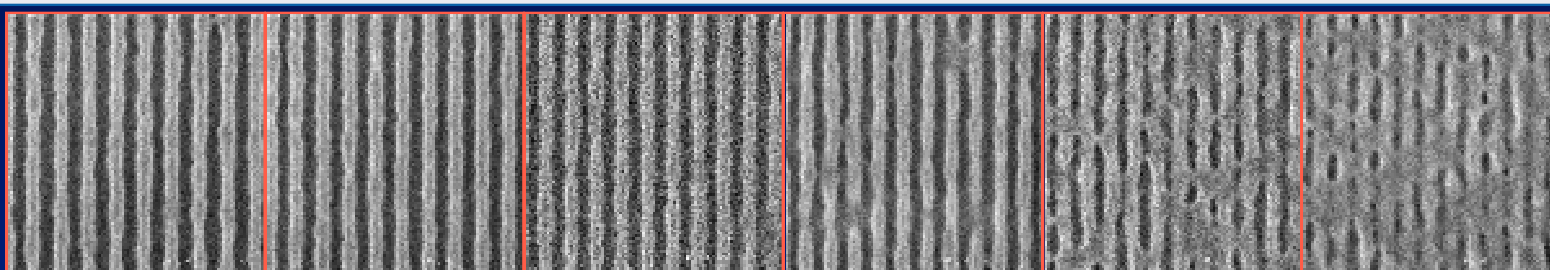
EUV1 0.25 NA Resolution with dipole illumination and Alt. PSM

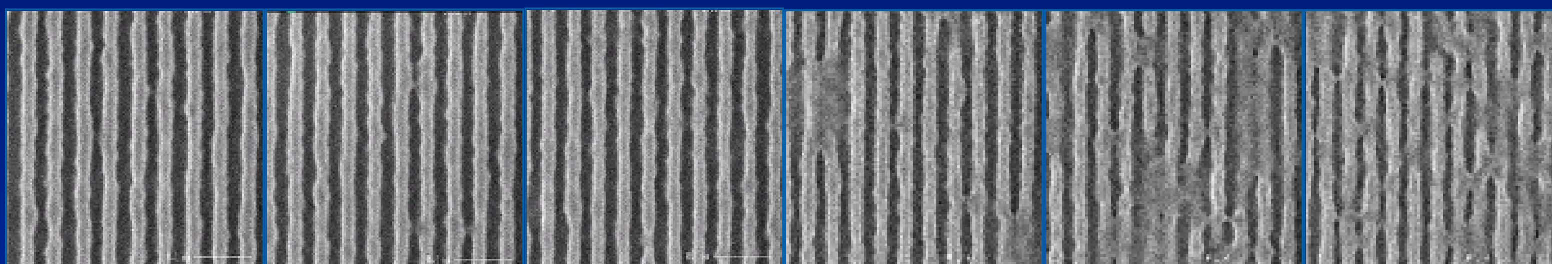
Target	24nm	23nm	22nm	21nm	20nm	19nm
CD	23.75	22.99	21.72	-	-	-
LWR	5.64	5.27	7.23	-	-	-
Dose	13	13	13	13	13	13

BIM C-Dipole



LWR reduction is needed for 22 nm HP

APSM Conv 0.3



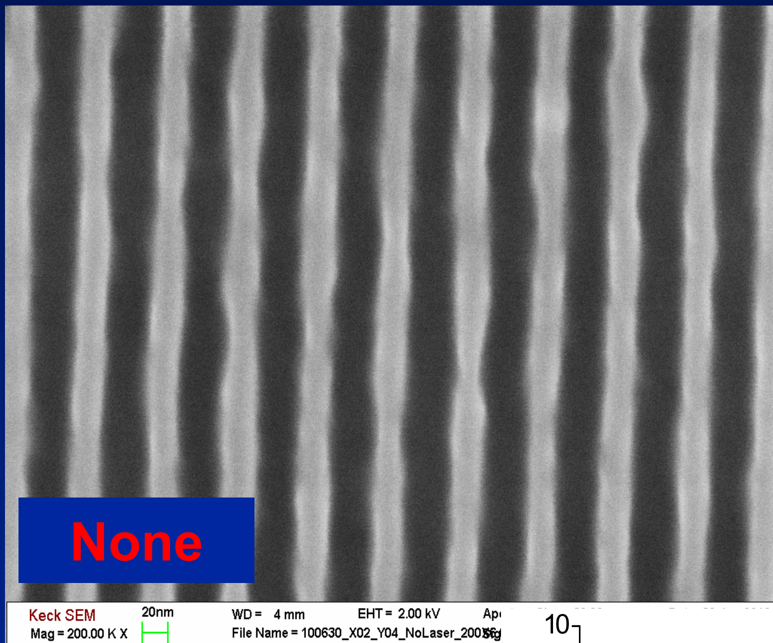
Target	24nm	23nm	22nm	21nm	20nm	19nm
CD	25.12	23.70	22.60	-	-	-
LWR	4.88	5.33	5.11	-	-	-
Dose	9.5	9.5	9.5	9.5	9.5	9.5

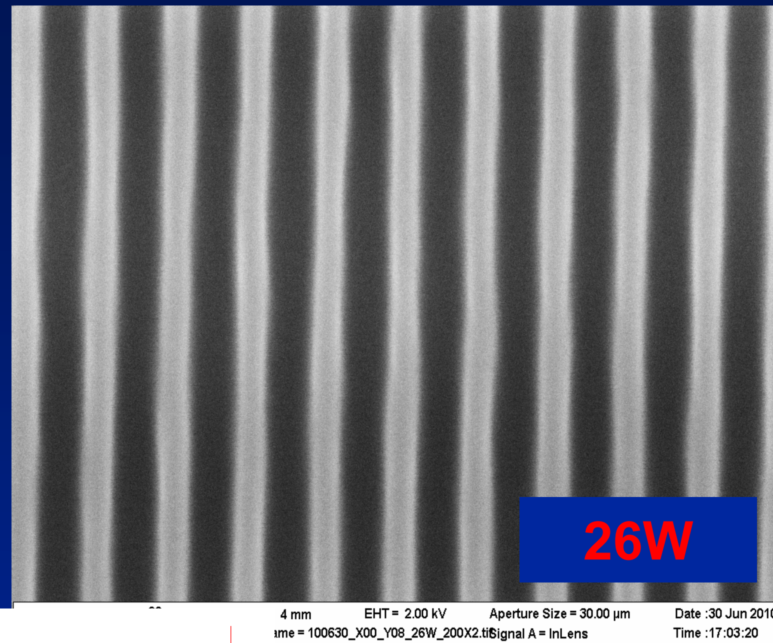
- Dipole imaging can be used to print 22 nm hp with 0.25 NA and binary masks
- While more work is needed in improving Alt. PSM, demonstration shows that PSM can play a significant role in enhancing EUV imaging

Application of hard-bake

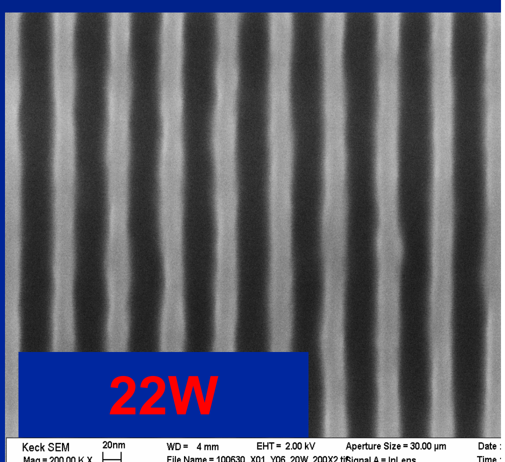
Laser anneal (LA), hardbake LWR reduction at 30 nm hp**

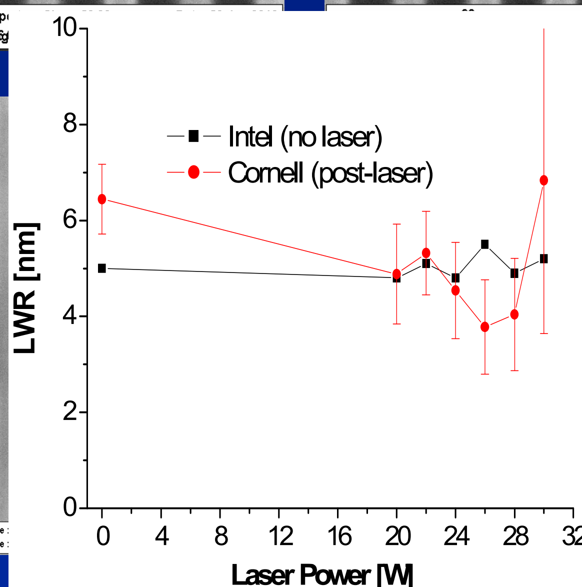
- Optimal smoothing* occurs in between 20W and 28W

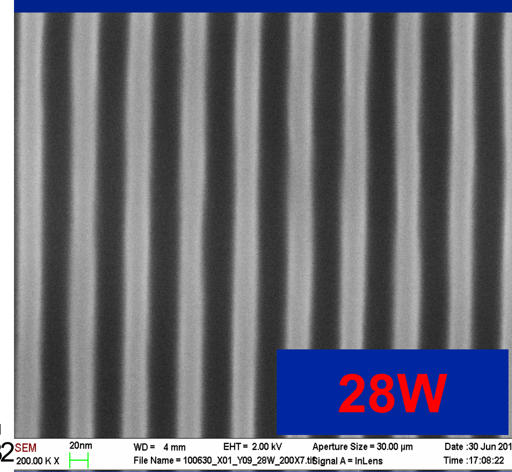




~ 30% reduction in LWR to 3 nm observed (@ 26W)





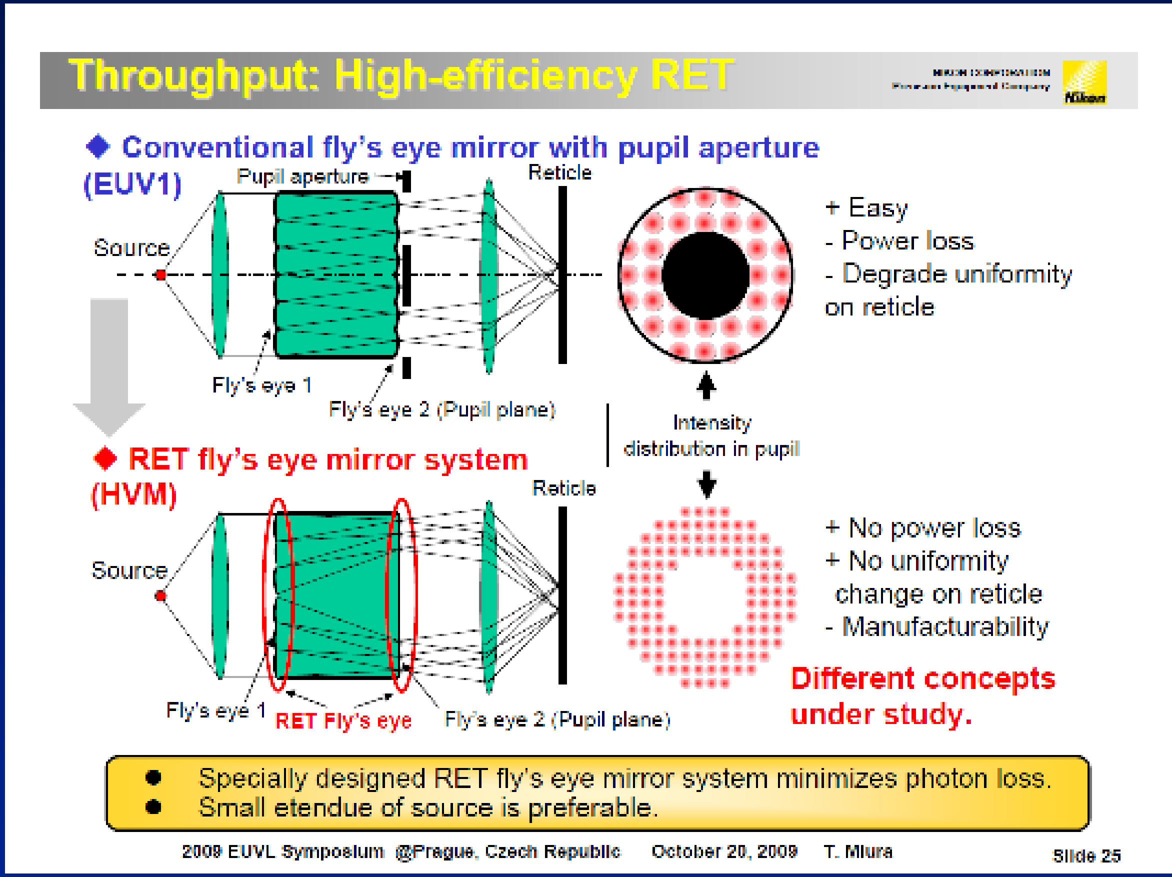


Upper limit; resist flow

* 5 images/measurement, analyzed by Summit™ s/w

**To be presented at SPIE 2011

High efficiency illuminators needed to enable OAI in HVM

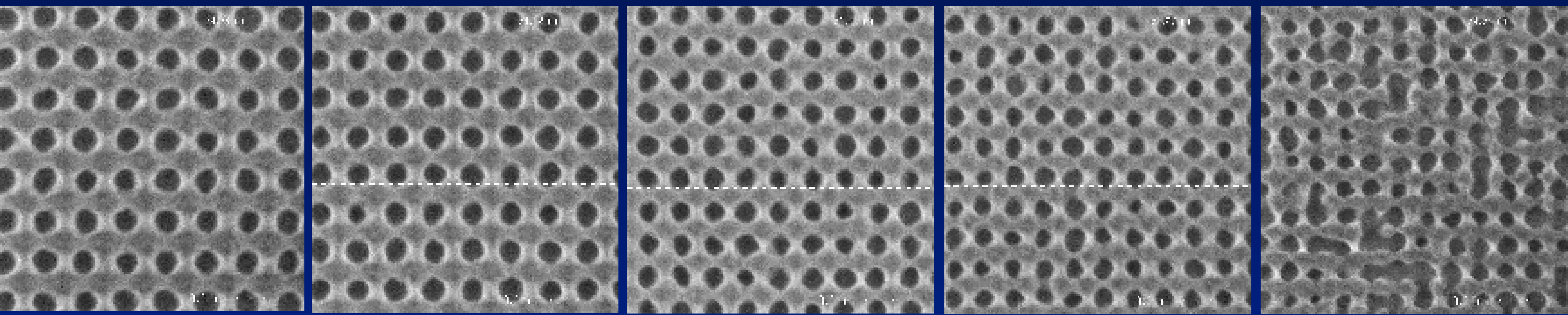


"Nikon EUVL Development Progress Update", T. Miura, 2009 EUVL Symposium

- HVM systems will be equipped with high efficiency off axis illuminators that minimize throughput loss
- DRs for P1274 will be set in Q3'2012 using 0.25 NA full field scanners
- So, 0.32 NA designs need to match the OAI settings w 0.25 NA to carry forward the early development

Contact Performance, Limited OPC
Quad Illumination, Intel-MET

30 nm hp | 28 nm hp | 24 nm hp | 22 nm hp | 20 nm hp



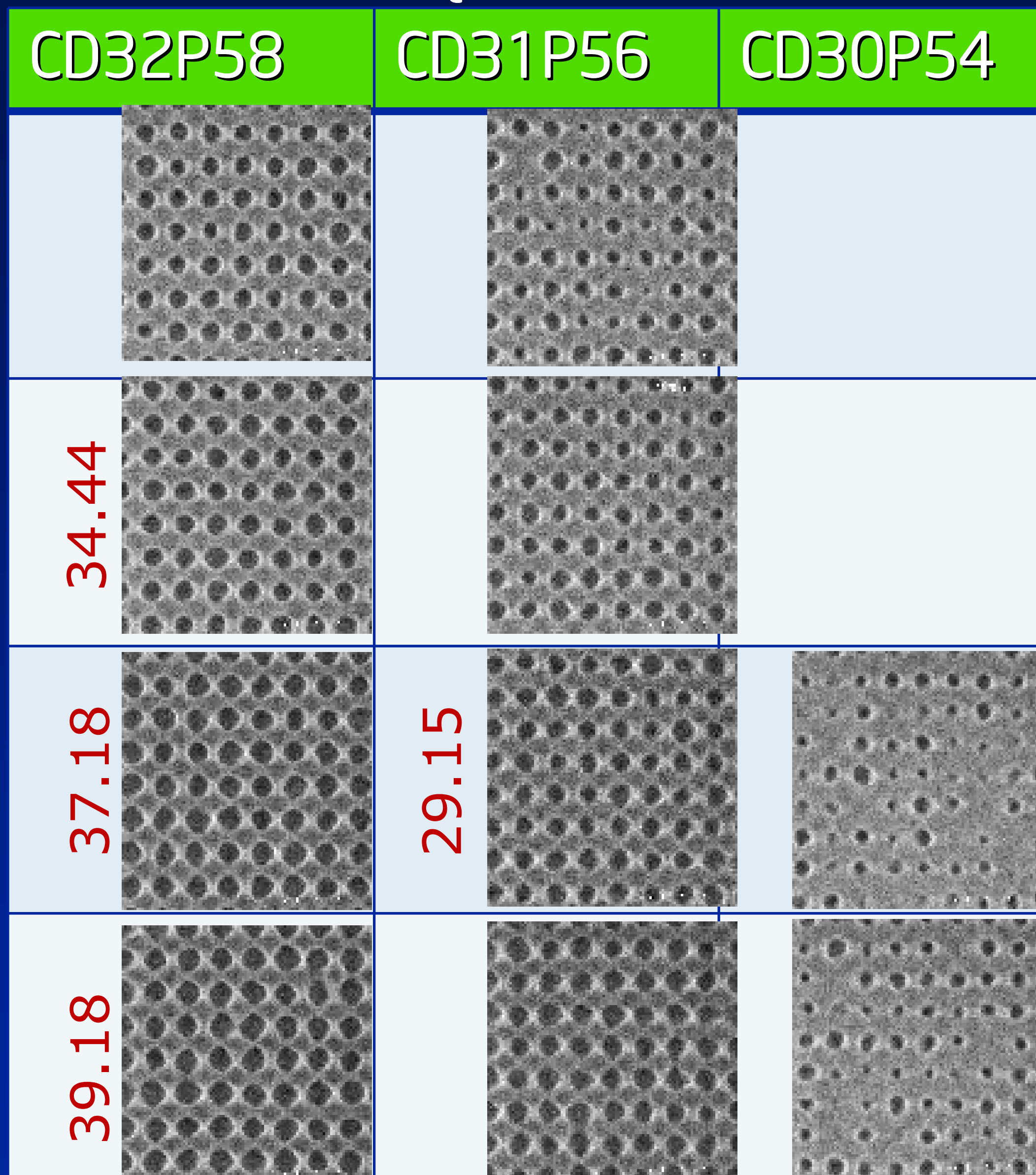
Resist R on UL A
FT = 50 nm

- Print bias ~8 nm (oversized contacts)

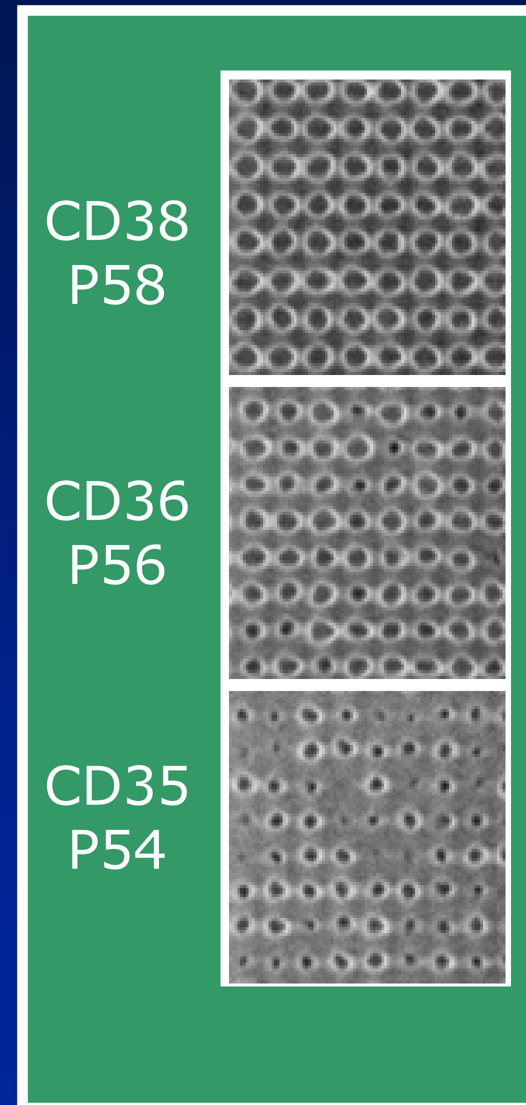
Good UR (~ 26 hp), but high Esize (22.5 mJ/cm^2)

Contact Holes, 0.25 NA resolution

EUV1 off-axis Quad illumination



ADT disk 0.5



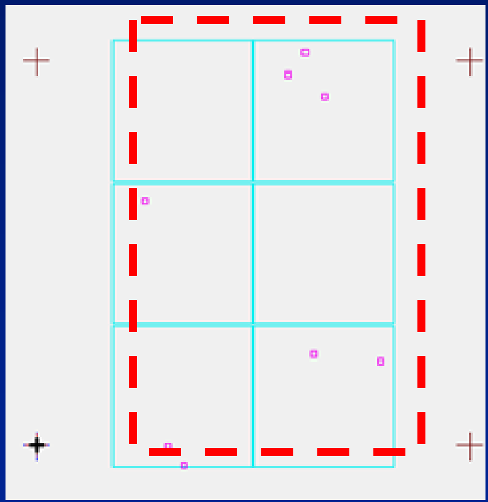
- Resolution improvement with EUV1 using quadrupole illumination (28 nm HP contacts resolved)

Corrections needed

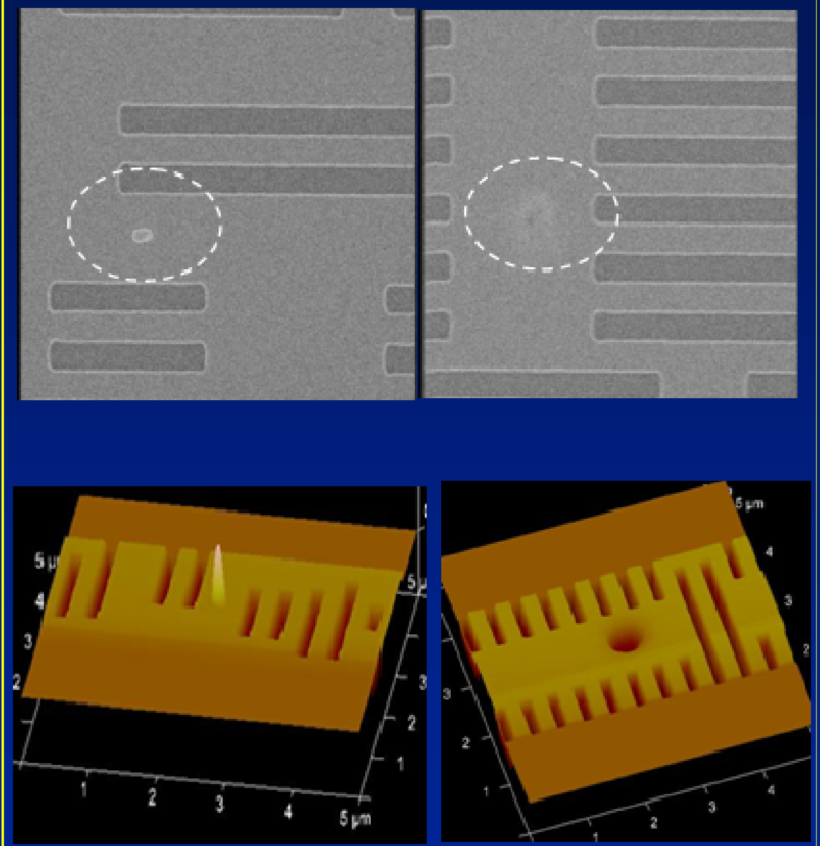
- Defect mitigation
- Flare induced CD variation
- Non-flatness induced overlay error
- HV bias shadowing
- OPC

Defect mitigation for large un-repairable defects

Defect mitigation by pattern shift

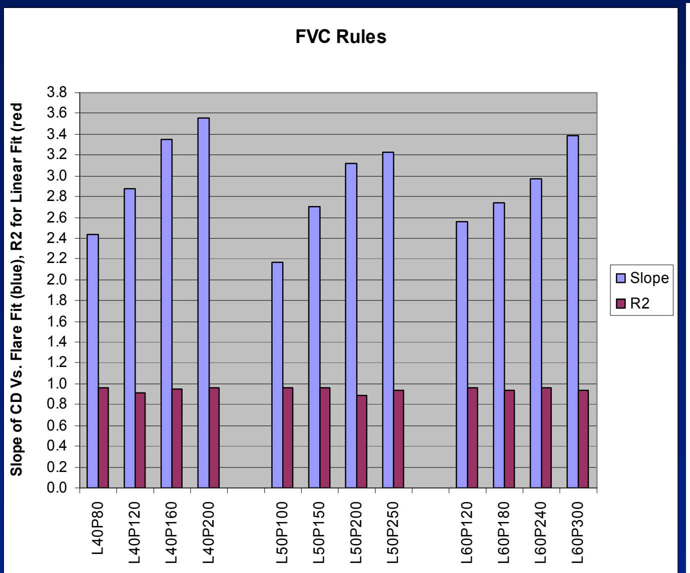
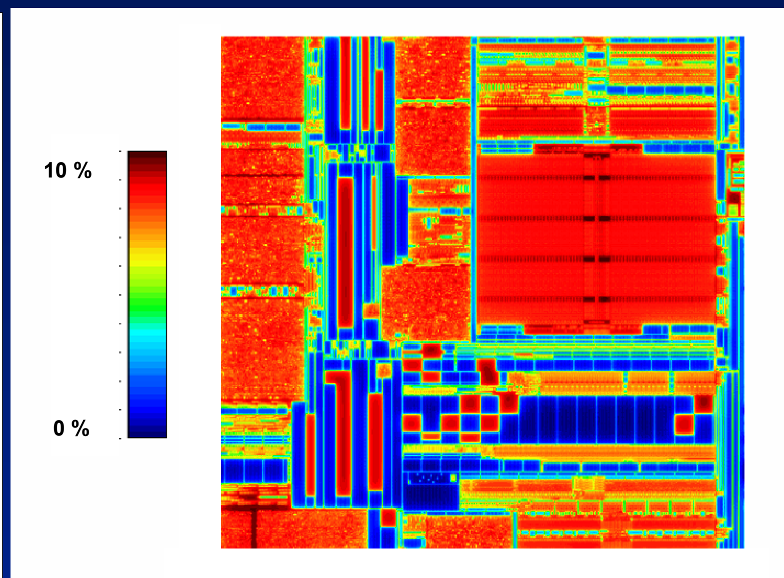
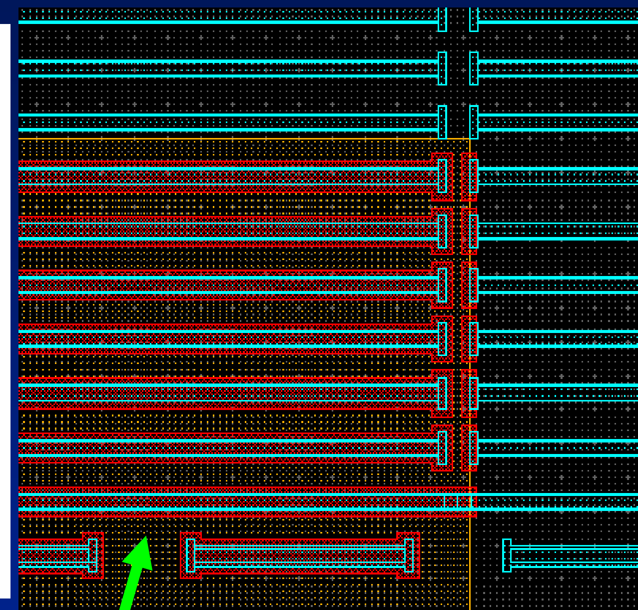


Note: Defects shown below are repairable



- Pattern shift calculated based on location within the field such that printable un-repairable defects are under large absorber areas will be applied
- Needs fiducial mark for reference

FVC (Flare Variation Compensation) – test result on mask design

ΔCD/ Δ Flare	Flare map	Post-FVC
		

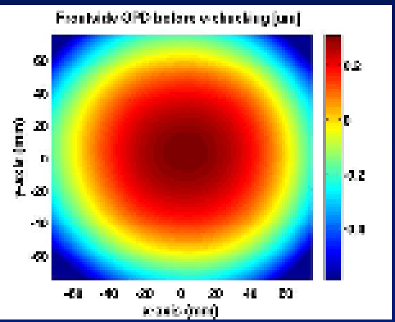
- All regions within the orange boundary get a bias depending on flare as per the equation below
- Model based FVC will be needed

$$CD_{new} = CD_{drawn} + \frac{\partial CD}{\partial Flare}\Big|_{Flare_{local}} \times \left(Flare_{nominal} - Flare_{local}\right) / MEEF$$

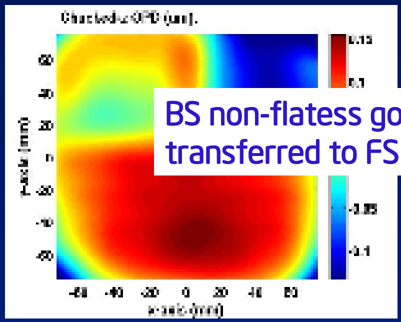
Overlay error in EUV masks due to e-chuck

Finite Element Modeling

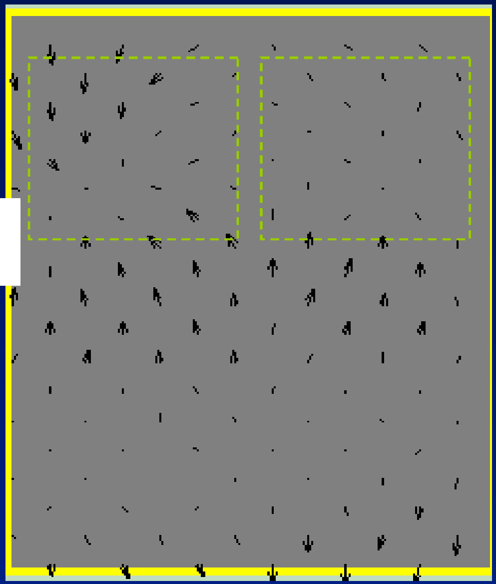
FS before e-chucking



FS after e-chucking

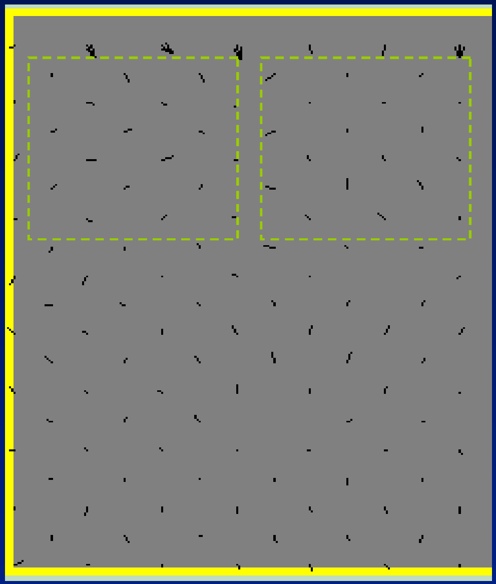


Uncompensated



Residual 3sigma
X=3.6nm
Y=9.1nm

Compensated

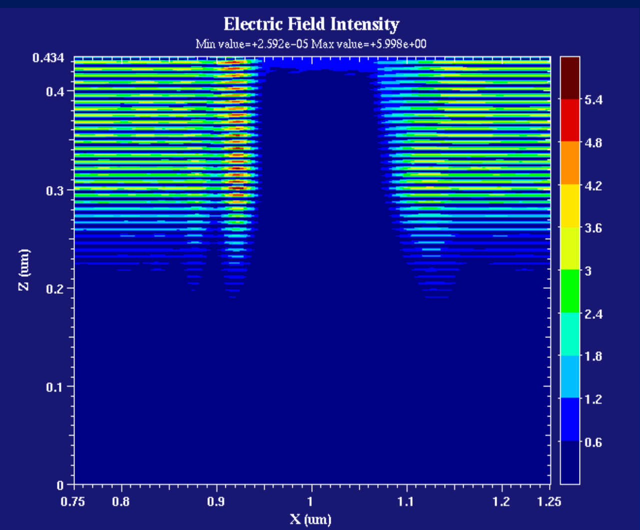


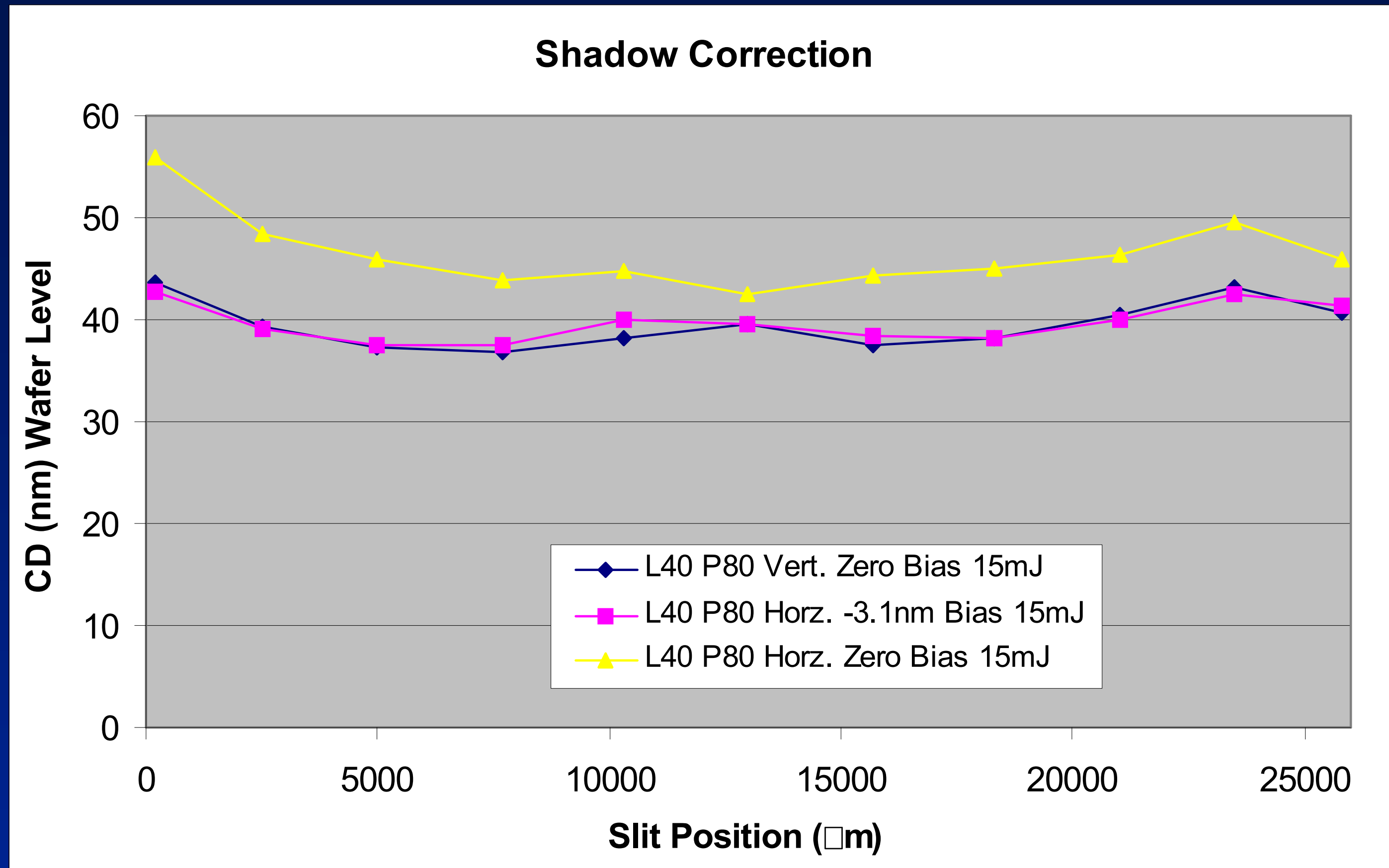
Residual 3sigm
X=4.3nm
Y=5.0nm

- Measure the FS & BS non-flatness of the mask
- Use a physically calibrated model of the e-chuck with the non-flatness data to compensate for OPD and IPD image placement errors using Ebeam Writer based Overlay error Correction (EWOC)
- The compensated map shows improvement in overlay

Mask Shadowing Compensation

E-field at mask





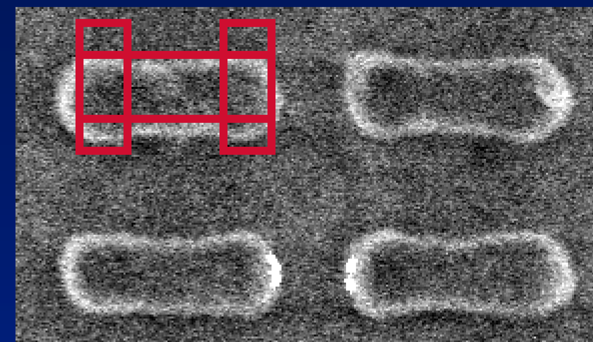
- Mask shadowing correction
  - Across slit variation will be compensated for based on Effective Shadowing Angle (ESA) variation across the slit modeled using rigorous thick mask simulator
  - CD H bias of -3.1 nm makes H-V bias = 0

OPC is needed for EUV

0 nm hammerhead

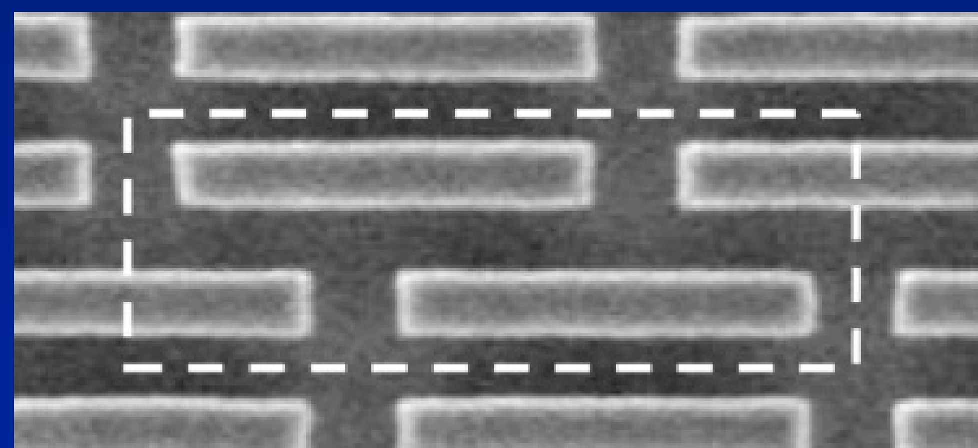
9 nm hammerhead

18 nm hammerhead



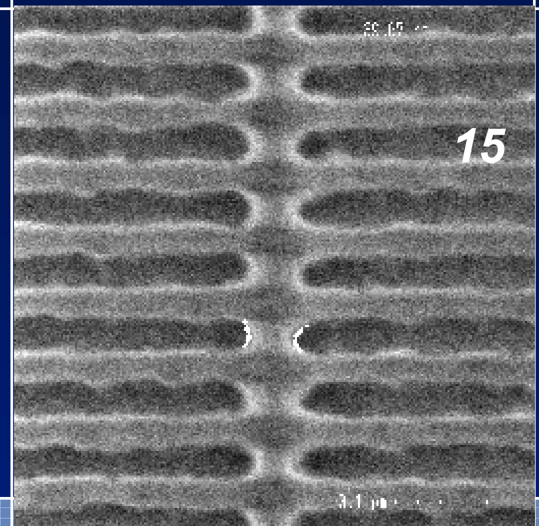
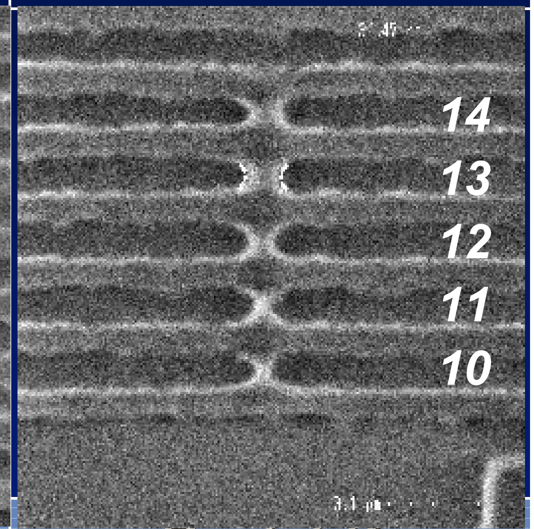
193 nm patterns set a high bar

193 nm patterned gates



- OPC needed for
  1. Proximity bias
  2. Corner rounding
  3. ETE pull-back

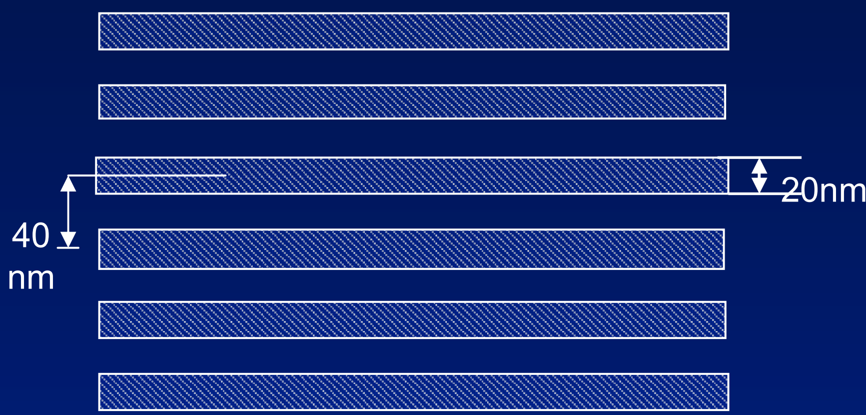
2D / ETE Performance :: Progress

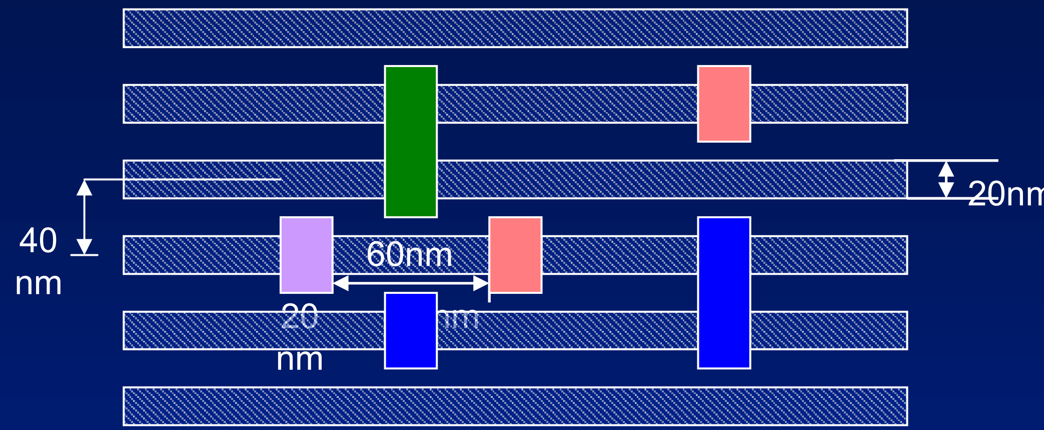
	2007	2008	2009/10
	Not Resolved ≤ 30 hp		
Resist	Resist S	Resist D	Resist K
Feature	30 nm hp	30 nm hp	30 nm hp
Min ETE	ND	40 nm	25 nm

- For 22 nm hp ETE patterning, no material progress possible until 0.32 NA tools are available
- Since the 0.32 tools are *not* going to be available in time for setting the DRs for 11 nm logic technology node (Q3'2012) , other alternatives need to be explored

11nm Logic Node* options

ArF Only Patterning





1 193i w/PD to form gratings + 4 193i Masks/Exposures to form Pattern = 5 Mask
5 Exposures

Complementary Patterning

CD, LWR <2nm 3s

CD, LWR <4nm 3s

1 Mask/1 193i Expose + 1 Mask/1 EUV Expose or 0 Mask/1 EBDW Expose

1 193i w/PD to form gratings + 1 EUV Masks/Exposure or 0 Mask/1 EBDW Exposure

Total 2 Masks/2 Exposures or 1 Mask/2 Exposures

*Y. Borodovsky, 2010 KLA Tencor Litho User Forum

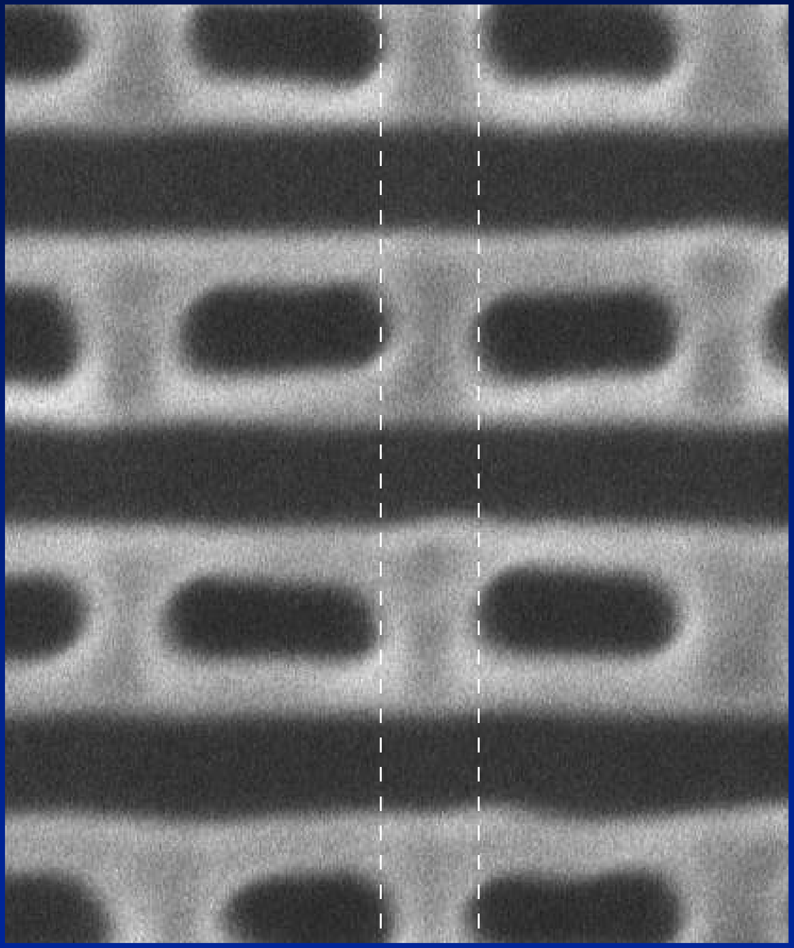
Advantages & disadvantages of complementary lithography

Using EUV to Break continuity of grating made by 193i with Pitch Division allows:

- - 2 Mask/ 2 Exposure per Critical Layer keeping all the benefits of mature 193i
- - Use of existing 0.25NA Tools for DRs generation
- - Use of higher sensitivity resists (LWR ~4 nm OK), hence higher TPT (same source)
- - Less Stringent EUV mask defect requirements
- - Lesser dependence on Actinic Inspection for EUV blanks and patterned masks
- - Higher success of blank defects mitigation techniques
- - Earlier start to EUV pilot line
- - Better chance for earliest EUV insertion into HVM

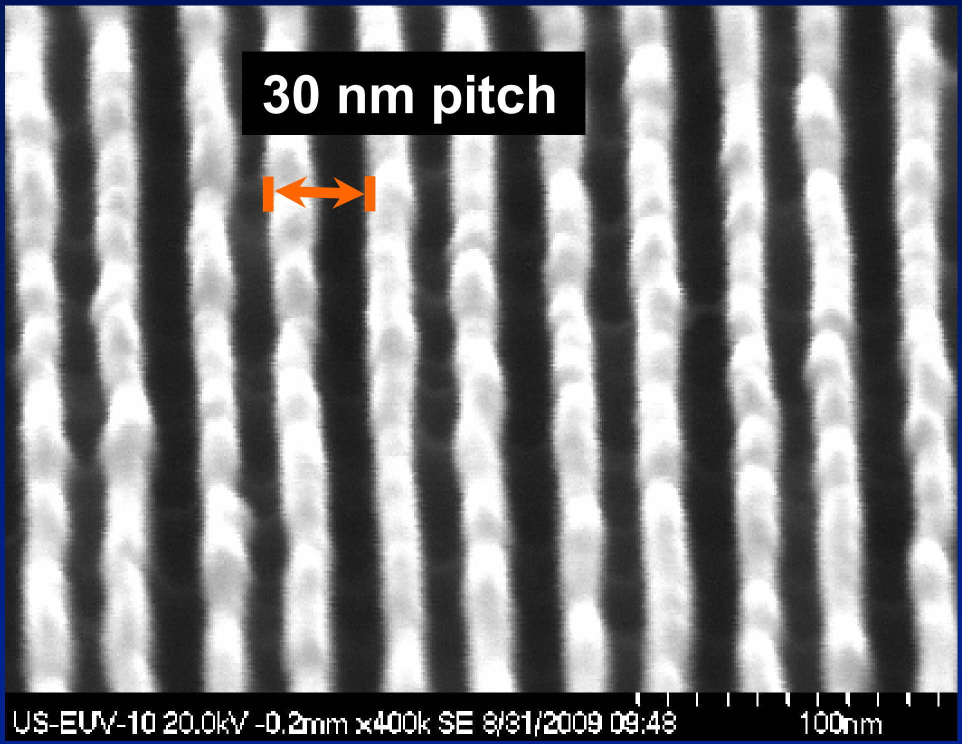
- However, it requires better mix-match overlay (EUV to 193 nm)

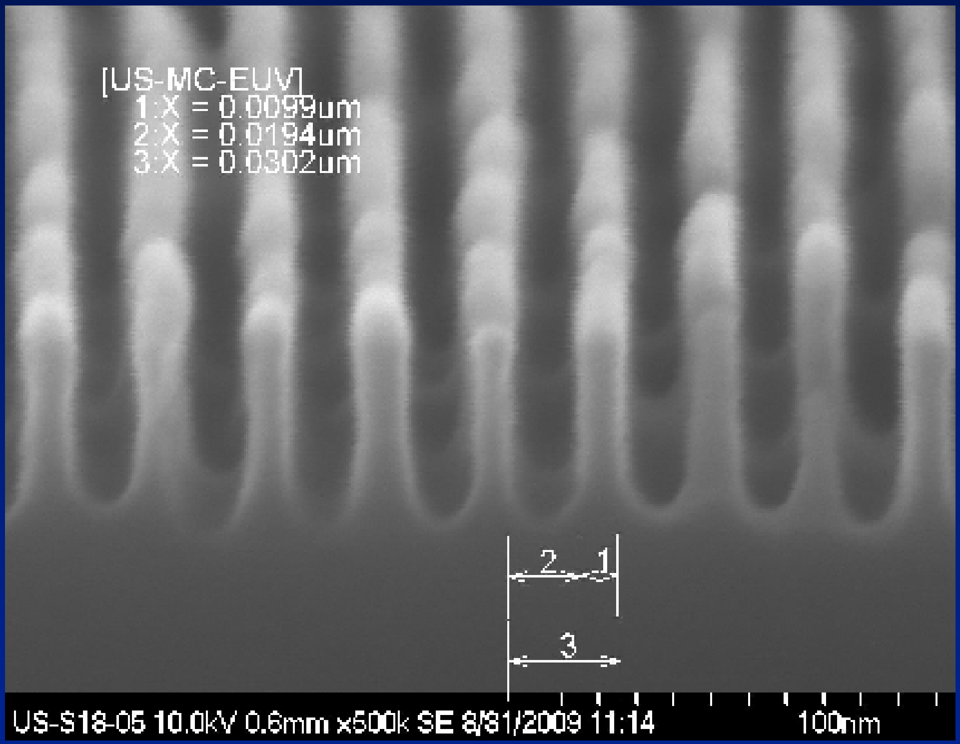
Sample Complementary lithography 22 nm hp 2D patterning



- Combination of 193 nm + EUV lithography and etch

Progress towards Sub 22 nm hp: 15 nm gratings with EUV





- Pitch halving a 30 nm hp grating made with EUV resist to achieve 15 nm hp
- Avoid pitch quartering with 193 nm

Summary

- While challenges remain for introduction into HVM, tremendous savings in complexity for 22 nm hp patterns can be achieved by using EUVL
- In 2011, a pilot line at Intel will be used to pattern critical layers either as a whole with EUV or in combination with 193 nm lithography using the complementary lithography approach
  - Corrections for optical proximity effects, flare, mask shadowing, mask defect mitigation, and mask non-flatness induced overlay, will be implemented
  - Photoresist performance improvements will be needed such as LWR for some critical layers

Acknowledgements

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- Cornell U
- IMEC
- SEMATECH